IN THE CLAIMS

What is claimed is:

1. A method for manufacturing a semiconductor device having an insulated gate field effect transistor (IGFET), comprising:

a first ion implantation step of implanting a first conductivity type impurity to form a first conductivity type high concentration source/drain shallow junction diffusion layer of a source/drain region of the IGFET using a gate electrode of the IGFET as an implant prevention mask; and

a second ion implantation step, after the first ion implantation step, of implanting a second conductivity type impurity to form a high concentration second conductivity type impurity diffusion layer for the source/drain region using the gate electrode as an implant prevention mask; wherein

the acceleration energy for the second conductivity type impurity is higher than the acceleration energy for the first conductivity type impurity of the first ion implantation step; and

an implant angle of the second conductivity type impurity with respect to a direction perpendicular to a (001) or equivalent face of a silicon substrate is in the range of 50°±6°.

2. The method of claim 1, wherein:

in the second ion implantation step, the silicon substrate is rotated while the implant angle is maintained with respect to the substrate.

3. The method of claim 1, wherein:

the first conductivity type is n-type and the second conductivity type is p-type

4. The method of claim 3, wherein:

the second conductivity type impurity is an indium (In) species.

5. The method of claim 3 wherein:

the first conductivity type impurity of the first ion implantation step is an arsenic (As) species.

6. The method of claim 1, further including:

an annealing step of activating at least the first conductivity type impurity of the first ion implantation step and the second conductivity type impurity.

7. The method of claim 6, wherein:

the annealing step is a rapid thermal anneal.

8. The method of claim 1, further including:

a third ion implantation step, after the second ion implantation step, of implanting a first conductivity type impurity to form another first conductivity

type diffusion layer at a greater depth than the high concentration second conductivity type impurity diffusion layer using the gate electrode and sidewalls formed on the sides of the gate electrode, as an implant prevention mask.

9. A method for manufacturing a semiconductor device, comprising the steps of:

forming a gate electrode on the surface of a semiconductor material having a cubic crystal structure; and

forming at least a portion of a source/drain region by implanting an impurity of a first conductivity type into a semiconductor crystal cubic structure at an inclination angle using the gate electrode as an implant mask while rotating the substrate about a rotational axis, wherein

the inclination angle is greater than 15° and less than 80° with respect to a direction perpendicular to the surface, and results in channeling of the impurity for a majority of directions about the rotating axis.

10. The method of claim 9, wherein:

the semiconductor crystal cubic structure comprises silicon; and

the inclination angle is in the range of 50°±6°.

11. The method of claim 9, wherein:

the impurity of a first conductivity type has a mass greater than arsenic (As).

12. The method of claim 9, wherein:

the impurity of a first conductivity type is a p-type impurity having a mass greater than boron (B).

13. The method of claim 9, wherein:

rotating the substrate about a rotational axis includes a rotation type selected from the group consisting of: continuous rotation and step rotation at predetermined angular intervals.

14. The method of claim 9, further including:

the step of forming at least a portion of a source/drain region includes,

prior to implanting the impurity of a first conductivity type, implanting an impurity of a second conductivity type with the gate electrode as an implant mask to form a high concentration source/drain shallow junction diffusion layer,

implanting the impurity of a first conductivity type forms a pocket implant diffusion region for preventing punch-through in an insulated gate field effect transistor comprising the gate electrode, and

a heat treatment step for activating the impurities of the first and second conductivity type.

15. The method of manufacturing a semiconductor device, comprising:

forming a gate electrode over a semiconductor substrate;

implanting an impurity of a first conductivity type at a first inclination angle with respect to a direction perpendicular to the substrate that avoids substantial channeling through a crystal structure of the semiconductor substrate with the gate electrode as an implant mask; and

implanting an impurity of a second conductivity type at a second inclination angle with respect to a direction perpendicular to the substrate that results in substantial channeling through the crystal structure of the semiconductor substrate with the gate electrode as an implant mask.

16. The method of claim 15, wherein:

the semiconductor substrate comprises a cubic crystal structure with a (001) or equivalent crystal face exposed to the implanting steps; and

the second inclination angle is in the range of 50°±6°.

17. The method of claim 15, wherein:

the semiconductor substrate comprises a cubic crystal structure with a (001) or equivalent crystal face exposed to the implanting steps;

the first inclination angle is in the range of 7-20°; and

the second inclination angle is in the range of 38-62°.

18. The method of claim 15, further including:

the step of implanting the impurity of the first conductivity type forms

a high concentration source/drain shallow junction diffusion layer of a source/drain region;

the step of implanting the impurity of the second conductivity type forms a pocket diffusion region for preventing punch-through of a transistor comprising the source/drain region and gate electrode; and

an annealing step for activating the impurities of the first and second conductivity types.

19. The method of claim 15, wherein:

the impurity of the second conductivity type has a mass less than the impurity of the first conductivity type.

20. The method of claim 19, wherein:

the first conductivity type is n-type; and

the impurity of the second conductivity type has mass greater than boron (B).